ABSTRACT

A digital PLL device in accordance with the present invention comprises a selector for selecting one of a first synchronous timing signal and a second synchronous timing signal, and a comparator for outputting a phase correction value corresponding to phase difference between the synchronous timing signal selected by the selector and an internal synchronous timing signal. The digital PLL device stores the phase correction value from the comparator at a stable operation. The digital PLL device also performs a hold over operation accompanied by high accurate phase correction based on the phase correction value, since a fault occurs in the first synchronous timing signal until the timing signal is switched to the second synchronous timing signal.